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EXAMINER	
NGUYEN, TOAN D	

ART UNIT	PAPER NUMBER
2472	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/225,388	SMITH, DAVID W	
	Examiner	Art Unit	
	TOAN D. NGUYEN	2472	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 September 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-18,20-28 and 30-35* is/are rejected.

7)☒ Claim(s) *7,19 and 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 November 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-35 have been considered but are moot in view of the new ground(s) of rejection.

The applicant argues on page 12, third paragraph with respect to claim 10, line 11 that an inadvertent typographical error was corrected (i.e., the spaces surrounding a previous amendment were underlined). The examiner disagrees. It is suggested the applicant corrects claim 10, line 11 by remove the underlined.

The applicant argues on page 13, second paragraph with respect to claim 23 that the language “a computer readable program storage device encoded with instructions” is fully support and enable by the Specification on page 4, lines 8-10 in the following passage: "The software must run to receive and process data packets, the processor, memory, and other major component of the computer, can not be placed into a true low-power mode.” The examiner disagrees. The Specification on page 4, lines 8-10 are in Description of the related art or prior art, and on page 8, lines 8-21, the specification discussed hardware circuitry to monitor incoming data. Claims 23-31 are rejected under 35 U.S.C. 112, first paragraph because the original disclosure supports only a statutory/hardware system with only a brief mention that such hardware system can be performed by various combinations of software and hardware without any adequate and enabling disclosure.

Claim Objections

2. Claim 10 is objected to because of the following informalities:

Claim 10, line 11, it is suggested to change "based_upon a content of_said data signal" to --- based upon a content of said data signal ---.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. Claims 23-31 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Regarding claim 23, the limitation "A computer readable program" was claimed. No support for this feature could be found in the original specification.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-2, 9, 23-24, 31-32, and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over McKaughan et al. (US 5,802,305) in view of Yamaura et al. (US 5,511,173).

For claim 1, McKaughan et al. disclose system for remotely waking a sleeping computer in power down state by comparing incoming packet to the list of packets storing on network interface card comprising:

receiving a set of data signals from an external data source (figure 4, col. 8, lines 45-47);

extracting a destination address from said set of data signals (col. 8, lines 47-50);

comparing said destination address extracted from said data signals to a known data value (col. 8, lines 52-54);

determining whether said received data signals should be received by a host circuitry based upon said comparison of said destination address extracted from said data signals to a known data value (col. 8, lines 54-58);

generating at least one status signal alerting said host circuitry of said determination that said received data signals should be received by said host circuitry (col. 8, lines 59-64); and

waking up said host circuitry from a sleep mode upon a determination that said received set of data is addressed to said host circuitry (figure 4, col. 8, lines 59-64).

However, McKaughan et al. does not expressly disclose detecting a size of said received set of data signals to use as a factor for decoding said data; and decoding said received set of data signals. In an analogous art, Yamaura et al. disclose detecting a size of said received set of data signals to use as a factor for decoding said data; and decoding said received set of data signals (col. 10, lines 24-29).

One skilled in the art would have recognized the detecting a size of said received set of data signals, and would have applied Yamaura et al.'s predecoder 33 in McKaughan et al.'s detects an incoming packet over the network. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use

Yamaura et al.'s programmable logic array and data processing unit using the same in McKaughan et al.'s system for remotely waking a sleeping computer in power down state by comparing incoming packet to the list of packets storing on the network interface card with the motivation being to provide the procedures for detecting the abbreviated instruction and the data size handled by the instruction (col. 10, lines 27-29).

For claims 2 and 24, McKaughan et al. disclose set of data signal received is data packet that is in a serial data format, over a network line (col. 8, lines 45-47).

For claims 9 and 31, McKaughan et al. disclose wherein said method of waking up said host circuitry further comprises generating a status signal alerting said host that a address match has been found (figure 4, col. 8, lines 59-62).

As far as understood with respect to claim 23, McKaughan et al. disclose system for remotely waking a sleeping computer in power down state by comparing incoming packet to the list of packets storing on network interface card comprising:

receiving a set of data signals from an external data source (figure 4, col. 8, lines 45-47);

extracting a destination address from said set of data signals (col. 8, lines 47-50);

comparing said destination address extracted from said data signals to a known data value (col. 8, lines 52-54);

determining whether said received data signals should be received by a host circuitry based upon said comparison of said destination address extracted from said data signals to a known data value (col. 8, lines 54-58);

generating at least one status signal alerting said host circuitry of said determination that said received data signals should be received by said host circuitry (col. 8, lines 59-64); and

waking up said host circuitry from a sleep mode upon a determination that said received set of data is addressed to said host circuitry (figure 4, col. 8, lines 59-64).

However, McKaughan et al. does not expressly disclose detecting a size of said received set of data signals to use as a factor for decoding said data; and decoding said received set of data signals. In an analogous art, Yamaura et al. disclose detecting a size of said received set of data signals to use as a factor for decoding said data; and decoding said received set of data signals (col. 10, lines 24-29).

One skilled in the art would have recognized the detecting a size of said received set of data signals, and would have applied Yamaura et al.'s predecoder 33 in McKaughan et al.'s detects an incoming packet over the network. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Yamaura et al.'s programmable logic array and data processing unit using the same in McKaughan et al.'s system for remotely waking a sleeping computer in power down state by comparing incoming packet to the list of packets storing on the network interface card with the motivation being to provide the procedures for detecting the abbreviated instruction and the data size handled by the instruction (col. 10, lines 27-29).

For claim 32, McKaughan et al. disclose system for remotely waking a sleeping computer in power down state by comparing incoming packet to the list of packets storing on network interface card comprising:

receiving a data signal (figure 4, col. 8, lines 45-47);

extracting said destination address based upon said data signal to determine whether a host circuitry is being addressed by comparing said destination address to a predetermined address; (col. 8, lines 47-54);and

waking up a host circuitry from a sleep mode based upon said determination that said host circuitry is being addressed (figure 4, col. 8, lines 59-64).

However, McKaughan et al. does not expressly disclose detecting a size of said received set of data signals to use as a factor for extracting a destination address. In an analogous art, Yamaura et al. disclose detecting a size of said received set of data signals to use as a factor for extracting a destination address (col. 10, lines 24-29).

One skilled in the art would have recognized the detecting a size of said received set of data signals to use as a factor for extracting a destination address, and would have applied Yamaura et al.'s predecoder 33 in McKaughan et al.'s detects an incoming packet over the network. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Yamaura et al.'s programmable logic array and data processing unit using the same in McKaughan et al.'s system for remotely waking a sleeping computer in power down state by comparing incoming packet to the list of packets storing on the network interface card with the motivation being to provide

the procedures for detecting the abbreviated instruction and the data size handled by the instruction (col. 10, lines 27-29).

For claim 34, McKaughan et al. disclose system for remotely waking a sleeping computer in power down state by comparing incoming packet to the list of packets storing on network interface card comprising:

receive a data signal (figure 4, col. 8, lines 45-47);

extract said destination address based upon said data signal to determine whether a host circuitry is being addressed by comparing said destination address to a predetermined address; (col. 8, lines 47-54);and

wake up a host circuitry from a sleep mode based upon said determination that said host circuitry is being addressed (figure 4, col. 8, lines 59-64).

However, McKaughan et al. does not expressly disclose detecting a size of said received set of data signals to use as a factor for extracting a destination address. In an analogous art, Yamaura et al. disclose detecting a size of said received set of data signals to use as a factor for extracting a destination address (col. 10, lines 24-29).

One skilled in the art would have recognized the detecting a size of said received set of data signals to use as a factor for extracting a destination address, and would have applied Yamaura et al.'s predecoder 33 in McKaughan et al.'s detects an incoming packet over the network. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Yamaura et al.'s programmable logic array and data processing unit using the same in McKaughan et al.'s system for remotely waking a sleeping computer in power down state by comparing incoming packet to the

list of packets storing on the network interface card with the motivation being to provide the procedures for detecting the abbreviated instruction and the data size handled by the instruction (col. 10, lines 27-29).

6. Claims 3-6, 8, 10-18, 20-22, 25-28, 30, 33, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over McKaughan et al. (US 5,802,305) in view of Yamaura et al. (US 5,511,173) further in view of Warren et al. (US 4,516,201).

For claims 3-6, 8, 25-28, 30, and 33, McKaughan et al. in view of Yamaura et al. do not expressly disclose:

converting said serial data packet into a parallel data format;

extracting a word clock from said received data packet;

incrementing a member held by said counter, said word clock generating a word count;

inputting said converted parallel format data into a plurality of comparators;

using said word count to address data stored in a memory circuitry; and

inputting a set of data signals from said memory circuitry into an appropriate comparator.

In an analogous art, Warren et al. disclose:

converting said serial data packet into a parallel data format (figure 2, col. 8, lines 23-28);

extracting a word clock from said received data packet (figure 5, col. 14, lines 14-16);

incrementing a member held by said counter, said word clock generating a word count (figure 6, col. 16, lines 1-52);

inputting said converted parallel format data into a plurality of comparators (figure 8, col. 23, lines 38-68);

using said word count to address data stored in a memory circuitry (col. 23, lines 3-5); and

inputting a set of data signals from said memory circuitry into an appropriate comparator (figure 8, col. 23, lines 38-68).

Warren et al. disclose further wherein said act of extracting a destination address from said set of data signals further comprises slicing said parallel data such that at least one destination address data word is generated (col. 8, lines 23-28 as set forth in claims 4 and 26); performing a comparison function upon said converted, parallel set of data signals, and said set of data from said memory circuitry (figure 8, col. 23, lines 38-68), generating a digital comparator status signal in response of said performance of comparator function; and clocking in said digital comparator data signal into a register (figure 8, col. 23, lines 27-68 as set forth in claims 5 and 27); determining whether said received data signals should be received by a host circuitry further comprises latching all output of said plurality of comparators into a digital logic circuitry (figure 2, col. 8, lines 23-28 as set forth in claims 6 and 28); performing an OR function upon all said latched output of said comparator (figure 7, col. 21, lines 33-38 as set forth in claims 8 and 30).

One skilled in the art would have recognized the converting said serial data packet into a parallel data format, and would have applied Warren et al.'s serial-to-parallel converter in McKaughan et al.'s detects an incoming packet over the network. Therefore, it would have been obvious to one of ordinary skill in the art at the time invention, to use Warren et al.'s multipled data communications using a queue in a controller in McKaughan et al.'s system for remotely waking a sleeping computer in power down state by comparing incoming packet to the list of packets storing on the network interface card with the motivation being to turn its serial input into selectably 5-bit or 8-bit parallel words (col. 8, lines 25-26).

McKaughan et al. disclose a plurality of comparators (figure 3, references 23 and 25, col. 5, lines 25-26).

For claims 10-18, 20-22, and 35, McKaughan et al. disclose system for remotely waking a sleeping computer in power down state by comparing incoming packet to the list of packets storing on network interface card, comprising:

means for receiving a data signal (figure 4, col. 8, lines 45-47);

a counter (col. 6, line 43);

a host circuitry interface capable of transmitting and receiving data from a host circuitry, said host circuitry enter a wake up state from a sleep mode based upon decoded address data received by said host circuitry, said decoded address data being base upon a content of said data signal and said size of said received data signals (figure 1, col. 6, lines 26-29);

a memory circuitry (figure 2, col. 6, lines 42-03);

a plurality of comparators (figure 8, col. 23, lines 38-68);

a mask circuitry (col. 8, line 48).

However, McKaughan et al. does not expressly disclose means for detecting a size of said received data signals. In an analogous art, Yamaura et al. disclose means for detecting a size of said received data signals (col. 10, lines 24-29).

One skilled in the art would have recognized the means for detecting a size of said received data signals, and would have applied Yamaura et al.'s predecoder 33 in McKaughan et al.'s detects an incoming packet over the network. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, to use Yamaura et al.'s programmable logic array and data processing unit using the same in McKaughan et al.'s system for remotely waking a sleeping computer in power down state by comparing incoming packet to the list of packets storing on the network interface card with the motivation being to provide the procedures for detecting the abbreviated instruction and the data size handled by the instruction (col. 10, lines 27-29).

Furthermore, McKaughan et al. in view of Yamaura et al. do not expressly disclose:

a data formatter;

a clock divider;

a digital logic circuitry;

a plurality of status registers and a plurality of clocked registers. In an analogous art, Warren et al. disclose:

a data formatter (figure 1, col. 6, lines 37-42);

a clock divider (col. 30, line 49);

a digital logic circuitry (figure 2, col. 8, lines 23-28);

a plurality of status registers and a plurality of clocked registers (figure 10, col. 30, lines 18-64).

Warren et al. disclose further formatter comprises of a serial to parallel converter and a data end detector that are capable of converting a serial stream of data into parallel data words and detecting an end of a data stream (figure 2, col. 8, lines 10-37 as set forth in claim 11); memory circuitry comprises of a memory element and a memory data access logic (figure 7, col. 12, lines 20-29 as set forth in claims 13 and 14); memory data access logic is coupled with said host interface such that data can be sent to and retrieved from said memory elements (figure 2, col. 8, lines 3-24 as set forth in claims 15 and 22); and comparators are coupled with said data formatter such that said comparators receive parallel formatted data from said data formatter (figure 8, col. 23, lines 38-68 as set forth in claims 16-18 and 20-21).

One skilled in the art would have recognized a data formatter, and would have applied Warren et al.'s data formatter in McKaughan et al.'s detects an incoming packet over the network. Therefore, it would have been obvious to one of ordinary skill in the art at the time invention, to use Warren et al.'s multipled data communications using a queue in a controller in McKaughan et al.'s system for remotely waking a sleeping computer in power down state by comparing incoming packet to the list of packets storing on the network interface card with the motivation being to provide the host with

status information concerning the data link, to inform the host, to take action when predetermined characters are received, to automatically generate the protocol characters required when transmitting and eliminate such characters when receiving (col. 6, lines 43-48).

Allowable Subject Matter

7. Claims 7, 19, and 29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to TOAN D. NGUYEN whose telephone number is (571)272-3153. The examiner can normally be reached on M-F (7:00AM-4:30PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Trost can be reached on 571-272-7872. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/T. D. N./

Examiner, Art Unit 2472

/Anh-Vu H Ly/

Primary Examiner, Art Unit 2472